UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,093	07/31/2001	Keith Rieken	I4303.0113	4453

38881 7590 04/25/2008

DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
04/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/920,093	RIEKEN ET AL.	
	Examiner	Art Unit	
	LILIAN VO	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13 and 16 – 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13 and 16 – 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 13 and 16 – 47 are pending. Claims 1 – 12 and 14 – 15 have been withdrawn.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/3/08 has been entered.

Election/Restrictions

3. This application contains claims 1 – 12 and 14 – 15 drawn to an invention nonelected without traverse in the reply filed on 3/7/06. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13 and 16 – 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belotserkovsky et al. (US 6,621,857, hereinafter Belotserkovsky) in view of Frank et al. (US 6,731,622, hereinafter Frank), further in view of Schuster et al. (US 6,591,355, hereinafter Schuster) and further in view of Cai et al. (6,349,363, hereinafter Cai).

6. As per **claim 13**, Belotserkovsky teaches the invention as claimed including a time-sliced processor for use in a communication system, comprising;

a master control unit including a time slot table (col. 1 lines 50-67; col. 8 lines 1-15; col.5 lines 45-67);

a symbol computing engine connected to an output of the data selector (col. 3 lines 29-55; col. 4 lines 46-67; col. 5 lines 19-40; col. 6 lines 39-55; col. 9 line 61- col. 10 line 40); and

a symbol integrator connected to an output of the symbol computing engine (col. 3 lines 29-55; col. 4 lines 46-67; col. 5 lines 19-40; col. 6 lines 39-55; col. 9 line 61- col. 10 line 40; col.4 line 64- col. 5 line 17; col. 7 lines 30-50).

Belotserkovsky did not clearly disclose partial sums search table, a data cache for receiving input data, a cache for receiving data from the data cache, a data selector connected to an output of the cache. Nevertheless, Frank discloses a partial sum table for any time slot granularity (fig. 9, col. 13 line 13 – col. 14 line 32) and Schuster discloses a data cache for receiving input data, a cache for receiving data from the data cache, a data selector connected to an output of the cache (col. 1 lines 25-50; col. 2 lines 29-39; col. 3 lines 11-25; col. 11 lines 45-65; col. 20 lines 30-40). In addition, Cai also teaches a data cache for receiving input data (col. 9 lines 16 – 24), a cache for receiving data from the data cache (col. 9 lines 16 – 24), a data

selector connected to an output of the cache (col. 11 lines 44 – 50, col. 9 lines 16 – 24). It would have been obvious for one of an ordinary skill in the art at the time the invention was made to combine the teachings of Cai, Frank and Scheuster together with Belotserkovsky to obtain a memory architecture that provides improved memory performance (Cai: col. 2 lines 1 – 2).

7. As per **claim 16,** as modified Belotserkovsky discloses the time-sliced processor, wherein the time-sliced processor is independent of a communication protocol (Schuster: fig. 1, col. 1 lines 30 – 50, col. 4 lines 53 – 67; col. 8 lines 44 – 65, col. 7 lines 14 - 35)

8. As per **claim 17**, as modified Belotserkovsky discloses the time-sliced processor is a spread-spectrum communication system (Belotserkovsky: col. 4 liens 25 – 45, col. 4 line 64 – col. 5 line 17, col. 7 lines 30 – 50, col. 10 line 40 – 65).

9. As per **claim 18**, as modified Belotserkovsky discloses the time-sliced processor is a supports multiple spread spectrum applications that run at different granularities when optimized (Schuster: fig. 1, col. 1 lines 30 – 50, col. 4 lines 53 – 67, col. 8 lines 44 – 65, col. 7 lines 14 – 35, col. 11 lines 50 – 65 and col. 19 lines 1 – 30).

10. As per **claim 19**, as modified Belotserkovsky discloses the time-sliced processor wherein the signal processing elements are finger processing elements (Schuster: col. 3 lines 29 – 55, col. 4 lines 46 – 67, col. 5 lines 19 – 40 and col. 6 lines 39 – 55).

11. As per **claim 20,** as modified Belotserkovsky discloses the time-sliced processor wherein the symbol computing engine is a despreader (Belotserkovsky: col. 3 lines 29 – 55, col. 4 lines 46-67; col. 5 lines 19-40; col. 6 lines 39-55; col. 9 line 61- col. 10 line 40).

12. As per **claim 21,** as modified Belotserkovsky discloses the time-sliced processor wherein the master control unit configures and controls the data cache and the signal processing elements (Belotserkovsky: col. 1 lines 30 – 49, col. 4 lines 25 – 45, 64 – col. 5 line 17, col. 7 lines 30 – 50).

13. As per **claim 22**, as modified Belotserkovsky discloses the time-sliced processor wherein the master control unit schedules time-sliced signal processing in the data cache and the signal processing elements (Belotserkovsky: col. 1 lines 50-67; col. 8 lines 1-15; col.5 lines 45-67).

14. As per **claim 23**, as modified Belotserkovsky discloses the time-sliced processor wherein the master control unit allocates time slots, maintains synchronization of the signal processing elements (Belotserkovsky: col. 1 lines 50-67; col. 8 lines 1-15; col.5 lines 45-67).

15. As per **claim 24**, as modified Belotserkovsky discloses the time-sliced processor wherein the master control unit allocates the partial sums search table on a per searcher basis to extend search control flexibility across time slots (Belotserkovsky: col. 1 lines 50-67; col. 8 lines 1-15; col.5 lines 45-67. Frank: fig. 9, col. 13 line 13 – col. 14 line 32).

16. As per **claim 25**, as modified Belotserkovsky discloses the time-sliced processor wherein the master control unit is linked to an external processing element to manage time slot allocation among the signal processing elements (Belotserkovsky: fig. 1, col. 1 lines 50-67; col. 8 lines 1-15; col.5 lines 45-67).

17. As per **claim 26**, as modified Belotserkovsky discloses the time-sliced processor calls programming across different protocols in a given application space (Schuster: fig. 1, col. 1 lines 30 – 50, col. 4 lines 53 – 67; col. 8 lines 44 – 65, col. 7 lines 14 - 35).

18. As per **claim 27**, as modified Belotserkovsky discloses the time-sliced processor performs speed grading of components (Schuster: fig. 1, col. 1 lines 30 – 50, col. 4 lines 53 – 67; col. 8 lines 44 – 65, col. 7 lines 14 - 35).

19. As per **claim 38**, as modified Belotserkovsky discloses the partial sum table completes a signal processing function across multiple time slots (Frank: fig. 9, col. 13 line 13 – col. 14 line 32).

20. As per **claim 39**, as modified Belotserkovsky discloses the data cache caches intermediate data for completing a signal processing function across multiple time slots (Schuster: col. 1 lines 25 - 50; col. 2 lines 29 - 39; col. 3 lines 11 - 25;col. 11 lines 45 -65; col. 20 lines 30 - 40).

21. **Claims 28 – 37 and 40 - 41** are rejected on the same ground as stated in claims 13 and 16 – 27 and 38 above.

22. As per **claims 42, 44 and 46**, as modified Belotserkovsky discloses the time slot granularity is at chip boundary (Frank: col. 2 lines 1 – 14, fig. 9, col. 13 line 13 – col. 14 line 32).

23. As per **claims 43, 45 and 47**, as modified Belotserkovsky discloses the time slot granularity is at sub-chip boundary (Frank: col. 2 lines 1 – 6, fig. 9, col. 13 line 13 – col. 14 line 32).

Response to Arguments

24. Applicant's arguments with respect to claims 13, 28 and 37 have been considered but are moot in view of the new ground(s) of rejection.

25. In response to applicant's argument that the references fail to show certain features of applicant's invention (page 11 paragraph 2), it is noted that the features upon which applicant relies (i.e., the caching at chip or sub-chip is essential to the claimed time-slice based processing which pauses an ongoing processing at time slice boundary, switches to some other processing, and resumes the processing later on by reloading the data in cache are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

26. With respect to applicant's remarks that "the claimed cache is accessed by a single computing device rather than multiple devices via a local area network" (page 11 paragraph 2), it is noted that applicant's disclosure states that data cache support two or more mobile terminal simultaneously (specification paragraph 35). In other words, the cache can be accessed by more than one computing device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

Lilian Vo
Examiner
Art Unit 2195